Claims

1. A method for forming a structure, the method comprising:

forming a layer over a substrate, the layer having a depletion region having a thickness less than approximately 20 angstroms;

removing a portion of the layer to define a gate of a transistor, the gate defining a channel length;

introducing a plurality of dopants into the substrate proximate the gate to define a source and a drain; and

heating the substrate to a temperature to activate the plurality of dopants,

wherein the temperature is sufficiently low to prevent at least a portion of the plurality of dopants from diffusing enough to induce a high off current.

2. The method of claim 1 wherein the substrate comprises an insulating layer.

3. The method of claim 2 wherein the substrate comprises a strained layer disposed over the insulating layer.

4. The method of claim 1 wherein the substrate comprises a strained layer.

5. The method of claim 4 wherein the strained layer is tensilely strained.

6. The method of claim 4 wherein the strained layer is compressively strained.

7. The method of claim 1 wherein the substrate comprises a relaxed layer.

8. The method of claim 1 wherein the substrate comprises germanium.

9. The method of claim 1 wherein the induced off current is less than 10^{-6} Amperes per micrometer.

10. The method of claim 9 wherein the induced off current is less than 10^{-9} Amperes per micrometer.

11. The method of claim 1 wherein after the plurality of dopants are introduced, a portion of the plurality of dopants disposed in a region of the source define a source extent proximate the channel, and after heating the substrate, the source extent diffuses under the gate a distance extending less than 12.5% of the channel length.

12. The method of claim 11 wherein a concentration of the portion of dopants at the source extent is at least approximately 10^{18} atoms/cubic centimeter.

13. The method of claim 1 wherein after the plurality of dopants are introduced, a portion of the plurality of dopants disposed in a region of the drain define a drain extent proximate the channel, and after heating the substrate, the drain extent diffuses under the gate a distance extending less than 12.5% of the channel length.

14. The method of claim 13 wherein a concentration of the portion of dopants at the drain extent at least approximately 10^{18} atoms/cubic centimeter.

15. The method of claim 1 wherein the layer comprises a semiconductor and the step of forming the layer includes introducing a plurality of gate dopants into the layer, and heating the layer to a first temperature to alter a distribution of the gate dopants in the layer.

16. The method of claim 15 wherein the semiconductor comprises silicon.

17. The method of claim 1 wherein the semiconductor comprises germanium.

18. The method of claim 1 wherein the layer comprises a metallic element.

19. The method of claim 18 wherein the metallic element comprises at least one of molybdenum, titanium, tantalum, tungsten, iridium, nickel, cobalt, and platinum.

20. A method for forming a structure, the method comprising:

introducing a first plurality of dopants into a gate electrode layer disposed over a substrate;

heating the gate electrode layer to a first temperature to alter a distribution of the first plurality of dopants in the gate electrode layer;

removing a portion of the gate electrode layer to define a gate of a transistor;

introducing a second plurality of dopants into the substrate proximate the gate to define a source and a drain; and

heating the substrate to a second temperature to activate the second plurality of dopants,

wherein the second temperature is less than the first temperature.

21. The method of claim 20 wherein the substrate comprises an insulating layer.

22. The method of claim 21 wherein the substrate comprises a strained layer disposed over the insulating layer.

23. The method of claim 20 wherein the substrate comprises a strained layer.

24. The method of claim 23 wherein the strained layer is tensilely strained.

25. The method of claim 23 wherein the strained layer is compressively strained.

26. The method of claim 20 wherein the substrate comprises a relaxed layer.

27. The method of claim 20 wherein the substrate comprises germanium.

28. The method of claim 20, wherein the first temperature is greater than 1000 °C.

29. The method of claim 20, wherein the second temperature is less than 1000 °C.

30. The method of claim 20 wherein the gate electrode layer comprises a semiconductor layer.

31. The method of claim 30 wherein the semiconductor layer comprises silicon.

32. The method of claim 30, wherein the semiconductor layer comprises germanium.

33. The method of claim 20 wherein the first plurality and the second plurality of dopants comprise n-type dopants.

34. The method of claim 20 wherein the first plurality and the second plurality of dopants comprise p-type dopants.

35. A method for forming a structure, the method comprising:

introducing a first plurality of dopants into a gate electrode layer disposed over a substrate;

heating the semiconductor layer for a first time period to alter a distribution of the first plurality of dopants in the gate electrode layer;

removing a portion of the gate electrode layer to define a gate of a transistor;

introducing a second plurality of dopants into the substrate proximate the gate to define a source and a drain; and

heating the substrate for a second time period to activate the second plurality of dopants,

wherein the second time period has a shorter duration than a duration of the first time period.

36. The method of claim 35 wherein the substrate comprises an insulating layer.

37. The method of claim 36 wherein the substrate comprises a strained layer disposed over the insulating layer.

38. The method of claim 35 wherein the substrate comprises a strained layer.

39. The method of claim 38 wherein the strained layer is tensilely strained.

40. The method of claim 38 wherein the strained layer is compressively strained.

41. The method of claim 35 wherein the substrate comprises a relaxed layer.

42. The method of claim 35 wherein the substrate comprises at least one of silicon and germanium.

43. The method of claim 35 wherein the first time period is greater than 5 seconds.

44. The method of claim 35 wherein the first time period is greater than 30 seconds.

45. The method of claim 35 wherein the gate electrode layer comprises a semiconductor layer.

46. The method of claim 45 wherein the semiconductor layer comprises silicon.

47. The method of claim 45 wherein the semiconductor layer comprises germanium.

48. The method of claim 35 wherein the first and the second plurality of dopants comprise n-type dopants.

49. The method of claim 35 wherein the first and the second plurality of dopants comprise p-type dopants.

50. A structure comprising:

a strained layer disposed over a substrate, and

a first transistor including:

a first source and a first drain, wherein at least a portion of the first source and a portion of the first drain are disposed in a first portion of the strained layer;

a first gate disposed above the strained layer and between the source and drain, the first gate comprising a first metal; and

a first gate dielectric layer disposed between the first gate and the strained layer.

51. The structure of claim 50 wherein the substrate comprises a dielectric material and the strained layer is disposed in contact with the dielectric material.

52. The structure of claim 50 wherein the first metal is selected from the group consisting of titanium, tungsten, molybdenum, tantalum, nickel, cobalt, and platinum.

53. The structure of claim 50 wherein the strained layer comprises silicon.

54. The structure of claim 50 wherein the gate comprises a metal-semiconductor alloy.

55. The structure of claim 54 wherein the gate consists essentially of the metal-semiconductor alloy.

56. The structure of claim 50, further comprising:

a channel disposed under the gate.

57. The structure of claim 56 wherein the source comprises a source extent proximate the channel, the source extent extending under the gate a distance less than 12.5% of a channel length.

58. The structure of claim 57 wherein a concentration of dopants in the source extent is at least approximately 10^{18} atoms/cubic centimeter.

59. The structure of claim 56 wherein the drain comprises a drain extent proximate the channel, the drain extent extending under the gate a distance less than 12.5% of a channel length.

60. The structure of claim 59 wherein a concentration of dopants in the drain extent is at least approximately 10^{18} atoms/cubic centimeter.

61. The structure of claim 50, further comprising:

a second transistor including:

a second source and a second drain, wherein at least a portion of the second source and a portion of the second drain are disposed in a second portion of the strained layer;

a second gate disposed above the strained layer and between the second source and second drain, the second gate comprising a second metal; and

a second gate dielectric layer disposed between the second gate and the strained layer,

wherein the first transistor is an n-type metal-oxide semiconductor field-effect transistor, the first source and the first drain comprise n-type dopants, the second transistor is a p-type metal-oxide-semiconductor field-effect transistor, and the second source and second drain comprise p-type dopants.

62. The structure of claim 61 wherein the first gate has a first workfunction, the second gate has a second workfunction, and the first workfunction is substantially equal to the second workfunction.

63. The structure of claim 61 wherein the first gate has a first workfunction, the second gate has a second workfunction, and the first workfunction is substantially different from the second workfunction.